REMARKS

Initially, in the Office Action dated April 8, 2005, the Examiner rejects claims 1-6 and 9-14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,683,533 (Shiozaki et al.) in view of U.S. Patent Publication No. 2002/0194435 (Yamagami et al.). Claims 7, 8 and 15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shiozaki et al. in view of Yamagami et al. and further in view of U.S. Patent No. 5,742,792 (Yanai et al.).

By the present response, Applicants have amended claims 9 and 15 to further clarify the invention. Claims 1-15 remain pending in the present application.

35 U.S.C. §103 Rejections

Claims 1-6 and 9-14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shiozaki et al. in view of Yamagami et al. Applicants respectfully traverse these rejections.

Shiozaki et al. discloses a storage control system that controls the update operations on two buffer address arrays in a data processing system in which a plurality of processors are connected to a shared storage, at least one of the processors having a buffer storage. The first buffer address array is the directory of buffer storage. The second buffer address array contains the same data as that of the first buffer address array. The storage control system updates first the content of the second buffer address array then that of the first buffer address array in response to a block transfer to the buffer storage of the own processor and a store operation conducted by other processor on the shared storage. The storage control

system permits to accept a new access request occurred in the own processor on condition that a block transfer to the own processor is finished and that the first buffer address array is updated in association with the block transfer.

Yamagami et al. discloses a storage control apparatus is coupled to a central processing unit (CPU) and a storage unit to control input/output of data between the CPU and the storage unit. The storage control apparatus has at least two processors coupled to the CPU and the storage unit, a cache memory (CM) unit for temporarily storing data of the storage unit, a shared memory (SM) unit for storing information concerning control of the CM unit and the storage unit, and a selector coupled to the at least two processors, the CM unit and the SM unit through access paths to selectively apply access requests from the at least two processors to the CM unit and the SM unit.

Regarding claims 1 and 9, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious many of the limitations in the combination of each of these claims. The Examiner asserts that Shiozaki et al. discloses a first control storage (address array) and a second control storage (address array) at col. 2, lines 1-3. However, this is not a first storage control apparatus or a second storage control apparatus, as recited in the claims of the present application. The address arrays disclosed in Shiozaki et al. are merely storage devices. An address array is not a control apparatus. Further, the address arrays disclosed in Shiozaki et al. do not receive a data input/output request from an information processing apparatus and perform a

data input/output process relative to a first storage volume or a second storage volume, as recited in the claims of the present application.

Further, none of the cited references disclose or suggest a first memory for storing data transferred between a first storage control apparatus and a second storage control apparatus. The Examiner appears to have failed to address these limitations in the claims of the present application, and has not asserted any portions of any reference that disclose these limitations.

In addition, none of the cited references disclose or suggest an input/output control unit for writing data transfer information in a second memory, the data transfer information containing a storage location of data in a first memory and a storage location of data in a second storage control apparatus. The Examiner asserts that these limitations are disclosed in Shiozaki et al. at col. 4, lines 9-13 and 19-26. However, these portions of Shiozaki et al. merely disclose, as the Examiner has partially noted, that a block transfer request received via line 13A is compared with an MS request from another processor to determine which has the higher priority and, therefore, if the block transfer request on line 13A will proceed. MS 3 is connected to other processors, i.e., 1B, that may also initiate block transfer requests. These portions of Shiozaki et al. do not disclose or suggest an input/output control unit for writing data transfer information in a second memory, the data transfer information containing a storage location of data in a first memory and a storage location of data in a second storage control apparatus, as recited in the claims of the present application. Shiozaki et al. merely discloses that a block transfer request

received from one processor is compared with requests from other processors to determine if it has the highest priority in order to proceed. Shiozaki et al. does not disclose or suggest writing data transfer information in a memory or data transfer information containing a storage location of data in a first memory and a storage location of data in a second storage control apparatus, as recited in the claims of the present application.

Moreover, none of the cited references disclose or suggest a data transfer control unit having a data buffer for storing data and a data transfer register for storing the data transfer information, the data transfer control unit controlling data transfer between a first memory and a second storage control apparatus in accordance with data transfer information read from the second memory and written in the data transfer register. The Examiner asserts that Shiozaki et al. discloses a first buffer address array as a buffer storage directory for registering thereto an address of data copied from a shared storage into a buffer storage of each processor and a second buffer address array provided for a store address check requested from another processor at col. 1, lines 8-15. However, this is not a data transfer control unit storing data and a data transfer register for storing data transfer information, where the data transfer control unit controls data transfer between a first memory and a second storage control apparatus, as recited in the claims of the present application. These portions of Shiozaki et al. merely disclose storing an address. These portions do not disclose or suggest anything related to controlling data transfer, or controlling data transfer between a memory and a second storage

control apparatus. Further, these cited portions or any other portions do not disclose or suggest controlling data transfer in accordance with data transfer information read from a second memory and written into a data transfer register.

In addition, none of the cited references disclose or suggest when a second data transfer based on second data transfer information is controlled while a first data transfer based on first data transfer information is controlled, the data transfer control unit writing the first data transfer information stored in the data transfer register and data in the data buffer into the second memory, reading the second data transfer information from the second memory, writing the second data transfer information in the data transfer register, and in accordance with the second data transfer information, controlling the second data transfer. The Examiner asserts that Shiozaki et al. discloses these limitations at col. 3, lines 31-36, col. 1, lines 25-27 and col. 2, lines 39-42. However, these portions merely disclose that access requests in the second processor is accepted when a transfer from the shared storage to the buffer storage of the second processor is completed and the first buffer address array is updated in association with the transfer. This is not when a second data transfer based on second data transfer information is controlled while a first data transfer based on first data transfer information is controlled, writing first data transfer information, reading second data transfer information, writing the second data transfer information, and controlling the second data transfer. According to the present invention, in contrast with Shiozaki et al., there is no requirement that the first transfer be completed.

The Examiner admits that Shiozaki et al. does not disclose or suggest a data transfer register for storing data transfer information but asserts that Yamagami et al. discloses these limitations. However, the cited portions of Yamagami et al. merely disclose that registers 340A and 340B are provided in correspondence to the respective shared memory access paths. However, this is not a data transfer register for storing data transfer information where the data transfer information contains a storage location of data in a first memory and storage location of data in a second storage control apparatus, as recited in the claims of the present application.

Regarding claims 2-6 and 10-14, Applicants submit that these claims are dependent on one of independent claims 1 and 9 and, therefore, are patentable at least for the same reasons noted previously regarding these independent claims. For example, Applicants submit that none of the cited references disclose or suggest where the data transfer is controlled in a unit of each data block contained by dividing data to be transferred between the first storage control apparatus and the second control apparatus into at least one or more data, or where the first storage control apparatus is connected to the second storage control apparatus in a communication enabled state via at least one or more switches.

Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of claims 1-6 and 9-14 of the present application. Applicants respectfully request that these rejections be withdrawn and that these claims be allowed.

Claims 7, 8 and 15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shiozaki et al., Yamagami et al. and further in view of Yanai et al. Applicants respectfully traverse these rejections.

Yanai et al. discloses remote data mirroring where two data storage systems are interconnected by a data link for remote mirroring of data. Each volume of data is configured as local, primary in a remotely mirrored volume pair, or secondary in a remotely mirrored volume pair. Normally, a host computer directly accessing either a local or primary volume, and data written to a primary volume is automatically sent over the link to a corresponding secondary volume. Each remotely mirrored volume pair can operate in a selected synchronization mode including synchronous, semi-synchronous, adaptive copy-remote write pending, and adaptive copy-disk. Direct write access to a second volume is denied if a "sync required" is set for the volume and the volume is not synchronized.

Regarding claim 8, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of this claim of, inter alia, a first storage control apparatus for receiving a data input/output request from an information processing apparatus and performing a data input/output process relative to a first storage volume for storing data and a second storage control apparatus connected to said first storage control apparatus in a communication enable state via at least one or more switches for performing a data input/output process relative to a second storage volume for storing data, or a cache memory unit having a circuit board

formed with a first memory for storing data transferred at least between said first storage apparatus and said information processing apparatus or said second storage control apparatus; or an input/output control unit for writing data transfer information in said second memory, said data transfer information containing a storage location of data in said first memory and a storage location of data in said information processing apparatus or said second storage control apparatus; or a channel control unit having a circuit board formed with a data transfer control unit, said data transfer control unit having a plurality of data buffers for storing data and a plurality of data transfer registers for storing said data transfer information, and controlling data transfer between said first memory and said information processing apparatus or said second storage control apparatus via said data buffer in accordance with said data transfer information read from said second memory and written in said data transfer register; or wherein, when a second data transfer based on second data transfer information is controlled while a first data transfer based on first data transfer information is controlled, said data transfer control unit reads said second data transfer information from said second memory, writes said second data transfer information into a second data transfer register, and in accordance with the second data transfer information, controls said second data transfer before said first data transfer information and data to be transmitted and received by said first data transfer are read from a first data transfer register storing said first data transfer information and a first data buffer storing the data to be transmitted and received by said first data transfer and written in said second memory.

As noted previously, neither Shiozaki et al. nor Yamagami et al. disclose or suggest these limitations in the claims of the present application. Moreover, Yanai et al. does not overcome the substantial defects noted previously regarding Shiozaki et al. and Yamagami et al.

Regarding claims 7 and 15, Applicants submit that these claims are dependent on one of independent claims 1 and 9 and, therefore, are patentable at least for the same reasons noted previously regarding these independent claims. For example, Applicants submit that none of the cited references disclose or suggest a channel control unit having a circuit board formed with said second memory, said input/output control unit and said data transfer control unit; a cache memory unit having a circuit board formed with said first memory; and a disk control unit for reading/writing data relative to said first storage volume, wherein: said first memory stores data to be transmitted and received at least between said first storage control apparatus and said information processing apparatus or said second storage control apparatus; said input/output control unit writes data transfer information in said second memory, said data transfer information containing the storage location of data in said first memory and a storage location of data in said information processing apparatus or said second storage apparatus; and said data transfer control unit controls data transfer between said first memory and said information processing apparatus or said second storage control apparatus via said data buffer in accordance with said data transfer information read from said second memory and written in said data transfer register

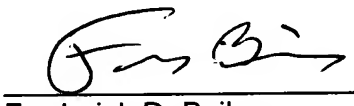
Accordingly, Applicants submit that none of the cited references, taken alone or in any proper combination, disclose, suggest or render obvious the limitations in the combination of each of claims 7, 8 and 15. Applicants respectfully request that these rejections be withdrawn and that these claims be allowed.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-15 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 500.43504X00).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



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